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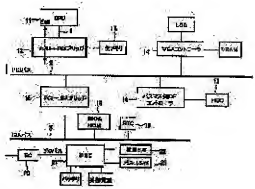
(54) COMPUTER SYSTEM AND DATA TRANSFER CONTROL METHOD

(57)Abstract:
PROBLEM TO BE SOLVED: To accelerate hibernation processing by using a data transfer mode that matches the performance of an operational hard disk drive and executing data transfer with the hard disk drive.
SOLUTION: When an event such as power switch off by a user occurs, the kind of a data transfer mode belonging to an HDD 17 is automatically discriminated before processing that saves content of a memory 3 in the HDD 17 and when the HDD 17 has a DMA mode, data transfer for memory data save is carried out in the DMA mode by using a bus master function of a bus master IDE controller 16. Then, it is possible to bring out the performance of the operational HDD 17 as much as possible and to realize the acceleration of hibernation processing.



CLAIMS

[Claim(s)]
[Claim 1]A computer system which is constituted so that wearing of a disk drive device is possible, and performs data transfer between said disk drive devices, comprising:
A means to distinguish a kind of data transfer mode which said disk drive device has by reading parameter information on the drive device from said disk drive device.
A transfer mode selecting means which chooses one data transfer mode from data transfer modes which said disk drive device has based on this discriminated result.
A data transfer control means which controls execution of data transfer between said disk drive devices using data transfer mode with this selected transfer mode selecting means.

[Claim 2]When a disk controller which has a bus master function is formed in said computer system, said transfer mode selecting means, When it distinguishes whether said disk drive device has DMA transfer mode and said disk drive device has DMA transfer mode, the DMA transfer mode is chosen and it does not have DMA transfer mode -- the computer system according to claim 1, wherein a case chooses high-speed data transfer mode which said disk drive device has in other transfer modes other than DMA transfer mode.
[Claim 3]The 1st data transfer control means by which said data transfer control means controls execution of data transfer between said disk drive device and a memory of said computer system using DMA transfer mode, Including the 2nd data transfer control means that controls execution of data transfer between said disk drive devices using other data transfer modes other than DMA transfer mode, in said 1st and 2nd data transfer control means, The computer system according to claim 1 or 2 characterized by a thing corresponding to data transfer mode with said selected transfer mode selecting means constituted so that a data transfer control means may be used for execution of said data transfer.
[Claim 4]A computer system for which it has a function which is constituted so that wearing of a disk drive device is possible, and saves the contents of the memory to a disk drive device at the time of shift to a power OFF state, comprising:
A means to distinguish a kind of data transfer mode which said disk drive device has by answering an event generation leading to power OFF, and reading parameter information on the drive device from said disk drive device.
A transfer mode selecting means which chooses one data transfer mode from data transfer modes which said disk drive device has based on this discriminated result.
A data transfer control means which performs data transfer from a memory of said computer system to said disk drive device, and saves the contents of said memory to said disk drive device using data transfer mode with this selected transfer mode selecting means.

[Claim 5]It is the data-transfer-control method used in a computer system which is constituted so that wearing of a disk drive device is possible, and performs data transfer between said disk drive devices, By reading parameter information on the drive device from said disk drive device, A kind of data transfer mode which said disk drive device has is distinguished, A data-transfer-control method choosing one data transfer mode from data transfer modes which said disk drive

device has based on this discriminated result, and controlling execution of data transfer between said disk drive devices using this selected data transfer mode.
[Claim 6]A disk controller which has a bus master function is formed in said computer system, When it distinguishes whether said disk drive device has DMA transfer mode and said disk drive device has DMA transfer mode, Control execution of data transfer between said disk drive devices using the DMA mode, have DMA transfer mode, and when there is nothing, A data-transfer-control method according to claim 5 controlling execution of data transfer between said disk drive devices using high-speed data transfer mode in other transfer modes other than DMA transfer mode.
[Claim 7]Are the data-transfer-control method used since the contents of the memory of the computer system are saved to a disk drive device at the time of power OFF of a computer system, and an event generation leading to power OFF is answered, By reading parameter information on the drive device from said disk drive device, A kind of data transfer mode which said disk drive device has is distinguished, Can lend in data transfer mode which said disk drive device has based on this discriminated result, choose one data transfer mode, and this selected data transfer mode is used, A data-transfer-control method performing data transfer from a memory of said computer system to said disk drive device, and saving the contents of said memory to said disk drive device.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention]This invention about the data-transfer-control method used with a computer system and a same system, It is related with the data-transfer-control method for improvement in the speed of the computer system which has a hibernation function which saves the contents of the memory to a hard disk drive especially at the time of power OFF, and its hibernation function.
[0002]
[Description of the Prior Art]In recent years, the personal computer of a portable notebook type or supplementary class note type and pocket computers, such as a Personal Digital Assistant, are developed variously.
[0003]In order that this kind of portable computer may extend the time in which battery-operated is possible, various power save modes (sleep mode) for saving the electric power of a computer system are provided. Suspend mode is one of the sleep modes with least power consumption. That is, when a computer system is suspend mode, power-off of almost all the devices of the others in a system excluding the main memory system data required for new starts, such as an operating system and a user program, are remembered to be is carried out.
[0004]The system data saved to main memory are the status of CPU just before a computer system is set as suspend mode, and the status of various peripheral LSIs. The user datum created by the operating system, and the run state of an application program and its application program is also memorized by this main memory. The information saved to main memory is used for restoration of the working state in front of suspend mode.
[0005]The save of system data is performed by the suspend routine included in system BIOS (intercalation output program). System BIOS is for controlling the hardware in a system according to the demand from an operating system, and contains the device driver group which controls the various hardware devices in a system. After the suspend routine of system BIOS is started at the time of the power OFF of a system, etc. and saves the register of CPU, and the status of various peripheral LSIs to a memory, it carries out power-off of the system.
[0006]As for the current supply to main memory, a system is maintained by a battery all the time during the power-off. For this reason, the status and user datum of a system can return a system to the working state before suspension at high speed, without disappearing.
[0007]However, if the capacity of a battery falls and it will be in a low battery state state when a system is in a suspend mode state, the data in main memory will disappear. In this case, the user datum which can return a system to the state before suspension and is developed by not only being lost but main memory will also disappear.
[0008]So, these days, hibernation mode is beginning to be used as a new sleep mode replaced with suspend mode. Hibernation mode is the mode to which power down of almost all the devices in the system containing main memory is carried out, after saving CPU, the status of various peripheral LSIs, the contents of main memory, etc. to a hard disk at the time of system power OFF.
Power consumption can be reduced rather than suspend mode.

Since the information saved to the hard disk does not disappear even if battery capacity falls, a system state can be normally restored to the state in front of hibernation mode. Therefore, many of portable computers with much use by the place where one has gone which cannot use an AC adapter mount hibernation mode as a sleep mode.

[0009]By the way, also in a portable computer, the memory space mounted as the main memory is in an increasing way with an operating system in recent years and the improvement in functional of an application program. If the storage capacity of main memory increases, the part, the time taken to save the contents of main memory to a hard disk, and the time taken to restore the contents of the hard disk to main memory will also increase. For this reason, in the system which uses hibernation mode. The time taken [after one / an electric power switch / the time taken / after the time which hibernation processing takes, i.e., a user, turns off an electric power switch / to actually carry out power-off of the system, and a user] to restore a system state is becoming very large.

[0010]In the former, data transfer between the hard disks performed at the time of the data save for a hibernation and restoration was always performed by PIO (Program I/O transfer) mode.

[0011]That is, in the portable computer, ATA (Enhanced IDE) is used as an interface used for connection of a hard disk drive. The typical transfer mode used by this Enhanced IDE is the above-mentioned PIO mode. It defines as ATA to PIO modes 0-4, and maximum transfer rates differ by it, respectively. In a PIO mode, it is the transfer mode which used the handshake of CPU and a hard disk drive, and when CPU repeats and accesses the I/O Port of a direct hard disk drive, data transfer is performed. Therefore, although that transfer rate was by no means high-speed, when the data transfer ability of the hard disk drive itself which needs seek operation and mechanical movement called rotation of a spindle was taken into consideration, this transmission mode was enough.

[0012]However, these days, the densification of a hard disk progresses quickly and data transfer ability's of the hard disk itself is improving substantially in connection with this, In addition to PIO mode 4 which was in use until now, a DMA mode and the hard disk drive further corresponding to UltraDMA mode are also beginning to be produced commercially. The hard disk drive is exchangeable by a user. For this reason, in the conventional hibernation processing of always performing data transfer using a PIO mode, the problem that that performance cannot fully be pulled out depending on the type of the hard disk drive currently used arises.

[0013]

[The issue which an invention will solve and to carry out] As mentioned above, even if it is the hard disk drive which is supporting fast transmission modes, such as a DMA mode, in the former, Transmission by a PIO mode will be performed and there was a problem that the performance could not fully be demonstrated depending on a hard disk drive in use. For this reason, much time is required in the hibernation processing which needs mass data transfer especially, There is a problem that the time taken [after one / an electric power switch / the time taken / after a user turns off an electric power switch / to actually carry out power-off of the system and a user] to restore a system state will become very large.

[0014]This invention is made in view of an above-mentioned situation, and it enables it to perform data transfer between the hard disk drive using the data transfer mode suitable for the performance of the hard disk drive in use, It aims at providing the data-transfer-control method used with the computer system and same system which can realize improvement in the speed of hibernation processing.

[0015]

[Means for Solving the Problem]In order to solve an above-mentioned technical problem, this invention is constituted so that wearing of a disk drive device is possible, and is characterized by that a computer system which performs data transfer between said disk drive devices comprises the following.

A means to distinguish a kind of data transfer mode which said disk drive device has by reading parameter information on the drive device from said disk drive device.

A transfer mode selecting means which chooses one data transfer mode from data transfer modes which said disk drive device has based on this discriminated result.

A data transfer control means which controls execution of data transfer between said disk drive devices using data transfer mode with this selected transfer mode selecting means.

[0016]By reading drive parameter information from a disk drive device with which it is equipped in this computer system, A kind of data transfer mode which the disk drive device has is distinguished automatically, and data transfer mode which should be used based on the discriminated result is chosen. Therefore, even if it is a case where what type of disk drive device is used, the maximum drawer ****** becomes possible about performance of a hard disk drive in use [the], and it becomes possible to aim at improvement in a data transfer rate.
[0017]When a disk controller with which this invention has a bus master function is formed in a computer system, When said transfer mode selecting means distinguishes whether said disk drive device has DMA transfer mode and said disk drive device has DMA transfer mode, The DMA transfer mode is chosen, it has DMA transfer mode, and when there is nothing, high-speed data transfer mode which said disk drive device has in other transfer modes other than DMA transfer mode is chosen. In a computer system which has by this a disk controller which has a bus master function, when using a disk drive device corresponding to DMA transfer mode, data transfer mode can be automatically set as DMA transfer mode.
[0018]This invention is constituted so that wearing of a disk drive device is possible, and it is characterized by that a computer system which has a function which saves the contents of the memory to a disk drive device at the time of shift to a power OFF state comprises the following.
A means to distinguish a kind of data transfer mode which said disk drive device has by answering an event generation leading to power OFF, and reading parameter information from said disk drive device.
A transfer mode selecting means which chooses one data transfer mode from data transfer modes which said disk drive device has based on this discriminated result.
A data transfer control means which performs data transfer from a memory of said computer system to said disk drive device, and saves the contents of said memory to said disk drive device using data transfer mode with this selected transfer mode selecting means.

[0019]In this computer system, if events, such as power supply switch off by a user, occur, Processing which saves the contents of the memory to a disk drive device is preceded, A kind of data transfer mode which a disk drive device has is distinguished automatically, and data transfer for a memory data save is performed using optimal data transfer mode in data transfer mode which the disk drive device has. Therefore, data transfer between the hard disk drive can be performed using data transfer mode suitable for the performance of a hard disk drive in use, and improvement in the speed of hibernation processing can be realized.
[0020]In a computer system which performs data save processing which this invention is constituted so that wearing of a disk drive device is possible, and saves the contents of the memory to a disk drive device at the time of shift to a power OFF state, Have CPU and a bus master function and A disk controller which can perform a DMA transfer between said disk drive device and said memory, An event generation leading to power OFF of said computer system is answered, A parallel control means to which parallel execution of data save processing by a DMA transfer which used said disk controller for said CPU, and the power down processing of various devices formed in said computer system is carried out is provided.
[0021]In this computer system, if events, such as power supply switch off by a user, occur, parallel execution of data save processing by a DMA transfer and the power down processing of various devices formed in a computer system will be carried out by CPU. In this case, while performing a DMA transfer using a disk controller, Since CPU is released from the data transfer processing, CPU resources can be assigned to power down processing called OFF of a display controller or a display, It becomes possible to shorten time taken [after a user turns off an electric power switch] to actually carry out power-off of the system.
[0022]Such parallel control prepares a processing program for two or more devices of every of a processing object containing a disk drive device, for example, and. And a counter value of two or more counters of each, which manage time required by shift to the next command processing

from the present command processing, is used, A means to detect timing which can shift to the next command processing for every device is prepared, That it can shift to the next command processing starts a control processing program corresponding to it in order from a detected device, and it makes the next command for the control management publish, And it is realizable by resetting a value of a counter corresponding to a device with which a command was published whenever a command was published.

[0023]

[Embodiment of the Invention]Hereafter, the embodiment of this invention is described with reference to drawings. The composition of the computer system concerning one embodiment of this invention is shown in drawing 1. This computer system is a notebook type or supplementary class note type portable personal computer, and comprises a computer body and a LCD panel unit attached to this computer body enabling free opening and closing. This computer has a built-in battery and is constituted by the electric power from that built-in battery so that operation is possible. Electric power supplies can also be received from external powers, such as AC commercial power, via an AC adapter. When having received the electric power supply from the external power, the electric power from the external power is used as operation power of a computer system. At this time, charge of a built-in battery is also automatically performed by the electric power from an external power. When an AC adapter is removed or the breaker of AC commercial power is dropped, the electric power from a built-in battery is used as operation power of a computer system.

[0024]The computer body is equipped with the hard disk drive (HDD) 17 which has an IDE interface, enabling free removal. This HDD17 is used as a secondary storage of a computer.

[0025]On the system board of this computer, Between CPU11, CPU bus 1, and PCI bus 2. Host PCI bridge 12 to connect, the main memory 13, VGA controller 14, PCI-ISA bridge 15, the busmaster IDE controller 16, BIOS-ROM18, the real-time clock (RTC) 19, an embedding controller. (EC) 20, the switch controller 21, etc. are formed.

[0026]CPU11 performs the motion control and data processing of this whole system. As this CPU11, what supports system management interruption SMI (SMI;SystemManagement Interrupt), for example, the microprocessor etc. which are manufactured and sold by U.S. Intel, "Pentium" is used. In this case, CPU11 has the following System Management Functions.

[0027]CPU11 as operational mode for executing programs, such as an application program and an operating system (OS), namely, a real mode, It has a protected mode and a virtual 8086 mode, and also has the operational mode for realizing the System Management Function called a System Management Mode (SMM;System Management mode).

[0028]A real mode is the mode which can access 1 M byte of memory space at the maximum, and conversion to a physical address from a logical address is performed by the address computation form of determining a physical address with the offset value from a base address expressed with a segment register.

[0029]On the other hand, a protected mode is the mode which can access a maximum of 4 G bytes per one task of memory space, and a linear address is determined using the address mapping table called a disk PURITA table. This linear address is eventually changed into a physical address by paging.

[0030]Thus, mutually different memory addressing is adopted in the protected mode and the real mode. A System Management Mode (SMM) is a false real mode, the address computation form in this mode of it is the same as the address computation form of a real mode, a disk PURITA table is not referred to, and paging is not performed, either. However, in SMM, the memory space over 1 M byte can be accessed like a protected mode.

[0031]When system management interruption (SMI;System Management Interrupt) is published by CPU11, the operational mode of CPU11 is switched to SMM from the real mode which is the operational mode at that time, a protected mode, or a virtual 8086 mode.When it switches to SMM by SMI, CPU11 saves the CPU status which is the contents of the CPU register at that time to SMRAM which is an overlay memory on the main memory 13. If return instruction (RSM command) is executed in SMM, CPU11 will restore CPU status from SMRAM to a CPU register, and will return to the operational mode before SMI generating. In this embodiment, the system

management program for performing hibernation processing etc. is executed in SMM. It is for this hibernation routine setting the system State as a suspend state or a hibernation state, In setting the system State as a hibernation state, After saving the contents of CPU11 and the State of various peripheral LSIs, the main memory 13, and the VRAM, etc. to the hibernation area beforehand secured in the storage area of HDD17, power-off of the whole system is carried out.
[0032]SMI in which this hibernation routine originates at system power OFF, That is, SMI generated by originating in the depression of the electric power switch 22, closing detection of the LCD panel unit by the panel switch 23, or the depression of a suspension button (sleep button) is answered, and it performs.
[0033]Although SMI is a kind of mask impossible interruption NMI, it is interruption of the degree of top priority whose priority is higher than usual NMI and maskable interrupt INTR. A system management program can be started by publishing this SMI, without being dependent on the application program under execution, or the environment of an operating system.
[0034]The circuit for performing control of the memory in a system and the whole I/O is built in host PCI bridge 12, and the hardware logic for SMI generating control is also incorporated here. This hardware logic comprises a status register holding the SMI generation circuit by a factor and SMI generation factor of others, such as an SMI generation circuit for starting hibernation processing, software SMI, and I/O trap SMI, etc.
[0035]An SMI generation circuit by switch controller 21 and EC20 course OFF of the electric power switch 22, When events, such as an LCD panel closing by the depression or the panel opening-and-closing pilot switch 23 of a suspension button, are notified, the SMI signal for starting hibernation processing is generated. The SMI signal from an SMI generation circuit is used also for the notice of the Wake rise event which directs the return from a hibernation state. That is, generating of the Wake rise event by one of the electric power switch 22 or LCD panel opening will perform restoration processing from a hibernation state to an operating state.
[0036]The main memory 13 is used as the main memory, i.e., the system memory, of this system, and the user datum etc. which were created by the operating system, the application program of a processing object, and the application program are stored. This main memory 13 is realized by semiconductor memory, such as DRAM. The above-mentioned SMRAM (System Management RAM) is the memory space assigned to a part of physical memory which constitutes the main memory 13, and only when an SMI signal is inputted into CPU11, a memory address is mapped and it becomes accessible. The address range by which SMRAM is mapped can be changed into the arbitrary places of 4-G byte space not with immobilization but with the register called SMBASE here. Unless a SMBASE register is among SMM, it cannot be accessed.
[0037]When CPU11 shifts to SMM, the register of CPU11 when CPU status, i.e., SMI, is generated, etc. are saved to SMRAM in stack form. The command for calling the system management program of BIOS-ROM18 is stored in this SMRAM. This command is a command executed first, when CPU11 goes into SMM, and control shifts from it to a system management program by this instruction execution.
[0038]BIOS-ROM18 is for memorizing system BIOS (Basic I/O System), and it is constituted by the flash memory so that program rewriting may be possible. System BIOS systematizes the function running routine for accessing the various hardwares in this system, and it is constituted so that it may operate in a real mode.
[0039]The IRT routine performed at the time of the power-on of a system, the BIOS driver group for various hardware control, etc. are contained in this system BIOS. Each BIOS driver contains two or more function running-routine groups corresponding to these functions, in order to provide an operating system and an application program with two or more functions for hardware control.
[0040]The system management program executed in SMM, such as an SMI hair drier and the above-mentioned hibernation routine, is also stored in BIOS-ROM18. When SMI which is for an SMI hair drier starting various SMI service routines according to the generation factor of SMI, and originates in power off operation occurs, A hibernation routine is started, and when SMI by other factors occurs, the SMI service routine corresponding to the factor is started.
[0041]Hibernation area is secured to a part of storage area of HDD17. Hibernation area is

secured by system BIOS at the time of initialization and the test of HDD17 by IRT, and other storage areas except hibernation area are released by OS. The field which continued physically is assigned to hibernation area.
[0042]RTC19 is a clock module and has the CMOS memory backed up by the original cell. Various system configuration information including the information etc. which specify upgrade mode is set to a CMOS memory.
[0043]EC20 is a controller for controlling the option which a system has, The thermal control function for performing the roll control of a cooling fan, etc. according to CPU ambient temperature etc., the various states of a system — lighting and the beep of LED — it has LED / beep sound control facility for one to inform a user, a power sequencing control facility which controls ON and OFF of system power, etc. in collaboration with the switch controller 21, a power supply status notice function, etc. A power supply status notice function is a function to supervise generating of the event which serves as a starting factor of the hibernation processing of system BIOS, or resume processing in collaboration with the switch controller 21, to use SMI etc. and to notify it to system BIOS at the time of an event generation. Also in a hibernation state, operation power is supplied to EC20 and the switch controller 21, and each function of EC20 is effective.
[0044]EC20 has an I/O Port for communication with system BIOS. System BIOS can perform setting out of the kind of event which should be supervised and notified, the lead of the status which shows the generated event, etc. by performing read/write to the configuration register in EC20 via this I/O Port. Communication between EC20 and the switch controller 21 is performed via I^2C bus.
[0045]For example, when there is battery residual quantity change, the switch controller 19 rewrites the configuration register of EC18 directly via I^2C bus. EC18 will be notified to system BIOS by making this into an event, if a configuration register is rewritten.
[0046]VGA controller 14 is for controlling LCD used as a display monitor of this system, and displays the picture data drawn by VRAM on LCD in a LCD panel unit.
[0047]The busmaster IDE controller 16 is for controlling the IDE device (here HDD17) with which the computer body was equipped, and supports the bus master function in which the DMA transfer between an IDE device and the main memory 13 can be performed. This bus master function performs the bus cycle for data transfer itself according to the command from CPU11, is in the state which reduced the CPU load rather than the PIO mode, and can carry out high speed execution of the data transfer between an IDE device and the main memory 13.
[0048]According to this embodiment, when equipped with the hard disk drive corresponding to a bus master, i.e., DMA transfer mode, data transfer for hibernation processing is performed by DMA transfer mode by using a bus master function. When equipped with the hard disk drive which does not support DMA transfer mode, auto select of the high-speed transfer mode in the transfer mode which the hard disk drive is supporting is made, and data transfer is performed in the transfer mode. When with what kind of transfer mode the hard disk drive deals reads the parameter information which shows it from a hard disk drive, it is distinguished automatically.
[0049]Next, with reference to drawing 2, a series of operations until a hibernation routine is started from generating of SMI are explained. If it is detected by the panel open/close switch 23 that the electric power switch 22 was turned off by the user working [a system], or the LCD panel unit was closed by the user, It is notified to an SMI generation circuit via EC20 that the power OFF factor generated the switch controller 21. This notice is answered, an SMI signal is generated from an SMI generation circuit, and it is supplied to CPU11.
[0050]If an SMI signal is inputted into CPU11, CPU11 will be switched to SMM from the operational mode at that time. If it goes into SMM, CPU11 maps a predetermined memory address in SMRAM first. Thereby, SMRAM becomes accessible.
[0051]The CPU state storage area, the hardware status (HW status) storage area which stores the status about other hardwares other than CPU, etc. are established in SMRAM, The jump code which specifies the SMI hair drier of BIOS-ROM18 as an interruption destination is set. As mentioned above, an IRT routine, an SMI hair drier, a hibernation routine, a resume routine, and

system BIOS containing two or more BIOS driver groups are stored in BIOS-ROM18.
[0052]Subsequently, CPU11 saves the CPU status (or called a context) which is the contents of the various registers of CPU11 when SMI is inputted in stack form to the CPU state storage area of SMRAM. And CPU11 fetches the code of the start address of SMM, i.e., the jump code set to SMRAM, and performs the SMI hair drier of BIOS-ROM18 specified in the jump code. The processing so far is performed by the micro program of CPU11 the very thing, i.e., CPU, 11.
[0053]The SMI hair drier called by execution of the jump code checks an SMI generation factor, in order to determine by what kind of factor SMI was generated. In this processing, the SMI status information set in the above-mentioned SMI status register is referred to. If it is SMI resulting from the power OFF leading to a suspension start, etc., an SMI hair drier will request execution of the hibernation routine of BIOS-ROM18. Thereby, a hibernation routine is performed in SMM and hibernation processing is started.
[0054]The method of the hibernation processing of this embodiment is shown in drawing 3. If the depression of power supply switch off, panel closing, and a suspension button, etc. are performed, the hibernation routine of system BIOS will be started and the following processings will be performed for system suspension.
[0055]That is, a hibernation routine saves system statuses, such as a register of CPU11, and status of various peripheral LSIs, etc. to the main memory 13 first (Step S101). Subsequently, HDD transfer mode decision processing for determining the data transfer mode between HDD17 is performed (Step S102). In this HDD transfer mode decision processing, the drive parameter information currently held there is first read from HDD17, and the kind of transfer mode which HDD17 is supporting is distinguished. And the optimal transfer mode that can most be transmitted at high speed is chosen in the transfer mode which HDD17 is supporting. Specifically, the transfer mode used by processing of drawing 4 is determined.
[0056]Based on drive parameter information, it is first judged whether HDD17 is supporting the Read/Write Multiple command as shown in drawing 4 (Step S301). A Read/Write Multiple command packs the read/write for two or more sectors, and is a command which can be specified, When this Read/Write Multiple command is not being supported, the data transfer mode using the Read/Write Sector command which specifies read/write per sector is used for HDD access. Next, it is judged whether DMA is supported or not from the HDD drive parameter read previously (Step S302). When not supporting, a Read/Write Multiple command is used for HDD access. It is a command of a Read/Write Sector command and a Read/Write Multiple command used by both in a PIO mode.
[0057]Next, it is judged whether Ultra DMA is supported from the HDD drive parameter read previously (Step S303). When not supporting, a DMA Read/Write command is used for HDD access. When supporting, a Ultra DMA Read/Write command is used. Thus, the kind of command is determined as the transfer mode and the concrete target which use it for HDD access. When an IDE controller is not a thing of bus master correspondence, what is necessary is to perform only Step S301, and the existence of a support of the DMA mode by Step S302 and S303 and the detection processing of a DMA mode currently supported become unnecessary.
[0058]Then, a hibernation routine carries out parallel execution of the data save processing to HDD, the power down processing of the various devices formed in the computer system, etc. These processings are performed by two or more serve routines prepared for every device, respectively, and the main routine in a hibernation routine performs processing which changes the command processing by these serve routine. That is, although a command is published one by one in the control management of each device, the waiting for I/O occurs in the degree of command issue. Therefore, the change of a serve routine is performed so that command issue processing to another device between the waiting for the I/O can be performed.
[0059]Here, HDD data save processing (Step S201), the I/O-hardware-control processing 1 (Step S202), the I/O-hardware-control processing 2 (Step S203) and -- I/O-hardware-control processing N (Step S204) -- it is alike, respectively, and it corresponds, the subroutine is prepared, and a main routine, Using the counter value (timer value) prepared for every device, the subroutine corresponding to the device which can shift to the next command processing is started, and the next command processing is performed (Step S103). And the command which

directs system power-off that all the processings including HDD data transfer processing are completed to EC20 is published (Step S105). (Step S104) Thereby, power-off of all the devices (main memory is included) except EC20 and the switch controller 21 is carried out, and the system State will be in a hibernation state.

[0060]As a subroutine which performs HDD data save processing, Read/WriteSector manipulation-routine #1 which performs data transfer control using a Read/Write Sector command like drawing 5, Read/WriteMultiple manipulation-routine #2 which performs data transfer control using a Read/Write Multiple command, DMA Read/Write manipulation-routine #3 which performs data transfer control using a DMA Read/Write command, UltraDMA manipulation-routine #4 which performs data transfer control using a Ultra DMA Read/Write command is prepared, and the manipulation routine corresponding to the transfer mode determined at Step S102 of drawing 3 is called and performed.

[0061]Next, with reference to drawing 6 and drawing 7, the operation in the case of advancing processing of two or more devices for a hibernation in parallel is explained using the comparison result of the counter value prepared for every device, and the counter value of a system counter.

[0062]Drawing 6 is a flow chart which shows the relation between the main routine of a hibernation routine, and a subroutine. Here, a hibernation routine assumes the case where it comprises a main routine and the three subroutines A, B, and C. The subroutine A is for carrying out power down of I/O device #1, such as a VGA controller and LCD, for example, answers the subroutine call from a main routine, and is started. The subroutine B is because memory data is saved to HDD17, answers the subroutine call from a main routine, and is started. The subroutine C performs power down processing of I/O device #2 of the communication system of USB, a modem, etc., for example, answers the subroutine call from a main routine, and is started.

[0063]the software counter (the I/O counter 1 and an HDD counter.) which looked the main routine like [I/O device#1, HDD, and I/O device #2], respectively, and was prepared by corresponding By comparing the counter value of the I/O counter 2 with turn with the present counter value by a system counter, the device which can shift to the next command processing is determined. And a corresponding-to the device subroutine is called.

[0064]The time which execution of the present command processing takes to a corresponding device, i.e., the time which can start the next command processing, is set to each software counter. Setting out of the counter value over each software counter is performed by the subroutine which controls the device corresponding to the software counter. The counter value over each software counter has become 0, i.e., the state where command processing can be started at any time, until a subroutine is started.

[0065]First, it is investigated whether a system current value is more than the value of the I/O counter 1 (Step S401), If a system current value is beyond the counter value of the I/O counter 1, the subroutine A will be called, and on the other hand, when a system current value is smaller than the counter value of the I/O counter 1, it shifts to the check of an HDD counter value.

[0066]Immediately after powering on, since the counter value of the I/O counter 1 is the initial value 0, a system current value is larger than the counter value of the I/O counter 1. Therefore, I/O-hardware-control processing 1 is performed by the subroutine A.

[0067]In the subroutine A, after the status check of command processing to the I/O command published by the last subroutine A is performed first, issue of the next command for the power down of I/O device 1 is performed. Subsequently, renewal of the counter value of the I/O counter 1 is performed.

[0068]Here, "the present system current value +n" is set as the I/O counter 1. "n" shows minimum time (interval value) until an I/O device ends the processing corresponding to the command published this time and it becomes receivable about the following command. It decides on this time beforehand for every command.

[0069]After renewal of the counter value of the I/O counter 1 finishes, it returns to a main routine. In a main routine, it is investigated whether a system current value is beyond an HDD counter value shortly (Step S402), If a system current value is beyond an HDD counter value, the subroutine B will be called and HDD data-transfer-control processing of the status check of

the last transfer command processing, issue of the following transfer command, the re set of an HDD counter, etc. will be performed.
[0070]When it returns from the subroutine B to a main routine, shortly, It is investigated whether a system current value is beyond the counter value of the I/O counter 2 (Step S403), If a system current value is a counter value of the I/O counter 2, the subroutine C will be called and processing of the status check of the last command processing, issue of the following command, the re set of the counter value of the I/O counter 2, etc. will be performed.
[0071]Thus, by using the counter value of each device, the timing which can shift to the next command processing is detected for every device, and processing to each device is advanced according to it.
[0072]When the DMA mode which uses a DMA Read/Write command and a Ultra DMA Read/Write command is used as HDD transfer mode, Since control of the DMA transfer from the memory 13 to HDD17 itself is performed by the busmaster IDE controller 16, The time which each command processing of the subroutine B takes can become short, CPU resources can be assigned to the meantime at power down processing of other I/O devices by the serve routines A and C etc., and improvement in the speed of the whole hibernation processing can be attained.

[0073]As mentioned above, in this embodiment, if events, such as power supply switch off by a user, occur, Data transfer for a memory data save is performed using the optimal data transfer mode in the data transfer mode which the kind of data transfer mode in which HDD17 has the contents of the memory 13 in advance of the processing saved to HDD17 is automatically distinguished, and the HDD17 has. Therefore, data transfer between the HDD17 can be performed using the data transfer mode suitable for the performance of HDD17 in use, and improvement in the speed of hibernation processing can be realized.
[0074]Also in the restoration processing from a hibernation processing state, same processing is performed and data transfer from HDD17 to the memory 13 is performed by the optimal transfer mode. In performing HDD access via system BIOS, at the time of the usual file access of application or OS, it becomes possible to perform data transfer between HDD17 by the optimal transfer mode.
[0075]
[Effect of the Invention]As explained above, according to this invention, data transfer between the hard disk drive can be performed now using the data transfer mode suitable for the performance of the hard disk drive in use, and the maximum drawer ****** becomes possible about the performance of a hard disk drive in use. Improvement in the speed of hibernation processing is realizable by enabling it to use a DMA mode automatically especially.

[Translation done.]